AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) A semiconductor device comprising:

a substrate having a semiconductor layer and a trench, said semiconductor layer being an epitaxial layer, said trench partitioning said semiconductor layer into a plurality of regions;

an element isolating insulating film provided in the trench for partitioning said semiconductor layer into **[[**an**]]** a plurality of element ~~region~~ regions, the element isolating insulating film having a top surface projecting upward above a top surface of said semiconductor layer, wherein the element isolating insulating film is an oxide film; and

a MOS type element formed within a corresponding one of the element regions and having a gate insulating film and a gate electrode on the gate insulating film, wherein:

a difference in height from the substrate between the top surface position of said element isolating insulating film and the top surface position of said semiconductor layer is at least three times as large as the thickness of said gate insulating film, the top surface position of said element isolating insulating film is not higher than a top surface position of the gate electrode, and said element isolating insulating film and said element regions make an interface which is substantially perpendicular to the top surface of said semiconductor layer.

2. (Currently Amended) A semiconductor device comprising:

a substrate having a semiconductor layer and a trench, said semiconductor layer being an epitaxial layer, said trench partitioning said semiconductor layer into a plurality of regions;

an element isolating insulating film provided in the trench for partitioning said semiconductor layer into **[[**an**]]** a plurality of element ~~region~~ regions, the element isolating insulating film having a top surface projecting upward above a top surface of said semiconductor layer, wherein the element isolating insulating film is an oxide film; and

a MOS type element formed within a corresponding one of said element regions and having a gate insulating film, wherein:

a difference in height from the substrate between the top surface position of said element isolating insulating film and the top surface position of said semiconductor layer is at least 10 nm, the top surface position of said element isolating insulating film is not higher than a top surface position of the gate electrode, and said element isolating insulating film and said element regions make an interface which is substantially perpendicular to the top surface of said semiconductor layer.

3. (Currently Amended) A semiconductor device comprising:

a substrate having a semiconductor layer and a trench, said semiconductor layer being an epitaxial layer, said trench partitioning said semiconductor layer into a plurality of regions;

an element isolating insulating film provided in the trench for partitioning said semiconductor layer into [[an]] a plurality of element ~~region~~ regions, the element isolating insulating film having a top surface projecting upward above a surface of said semiconductor layer; and

a MOS type element formed within a corresponding one of said element ~~region~~ regions and having a gate insulating film and a metal gate electrode formed thereon, wherein:

said gate insulating film ~~and said gate electrode are~~ is formed on a top surface and sides of the semiconductor layer in said element ~~region~~ regions which are not covered with said element isolating insulating film, said gate electrode is formed on said gate insulating film, and the top surface position of said element isolating insulating film is not higher than a top surface position of the gate electrode, and said element isolating insulating film and said element regions make an interface which is substantially perpendicular to the top surface of said semiconductor layer.

4. (Currently Amended) A semiconductor device according to claim 3, wherein the difference in height from said substrate between the top surface position of said semiconductor layer and the top surface position of said element isolating insulating film is at least ~~five~~ three times as large as a thickness of said gate insulating film.

5. (Original) A semiconductor device according to claim 3, wherein the MOS element includes a source/drain region and the difference in height from said substrate

between the top surface position of said semiconductor layer and the top surface position of said element isolating insulating film is substantially at least a junction depth of said source/drain region.

Claims 6-33. (Canceled)

34. (Previously Presented) A semiconductor device according to claim 3, wherein said element isolating insulating film and said gate insulating film are formed in different steps.

35. (Currently Amended) A semiconductor device according to claim 1, wherein said element isolating insulating film is a thermally grown oxide film~~, and said element isolating insulating film and said element region make an interface which is substantially perpendicular to a top surface of said semiconductor layer~~.

36. (Currently Amended) A semiconductor device according to claim 2, wherein said element isolating insulating film is a thermally grown oxide film~~, and said element isolating insulating film and said element region make an interface which is substantially perpendicular to a top surface of said semiconductor layer~~.

37. (Currently Amended) A semiconductor device according to claim 3, wherein said element isolating insulating film is a thermally grown oxide film~~, and said element isolating insulating film and said element region make an interface which is~~

~~substantially perpendicular to a top surface of said semiconductor layer~~.

38. (Currently Amended) A semiconductor device according to claim 1, ~~further comprising~~ wherein the gate electrode is a metal gate electrode formed on the gate insulating film, said gate insulating film being formed on a top surface and sides of the semiconductor layer in said element regions which are not covered with said element isolating insulating film, and said metal gate electrode being formed on ~~a top surface and sides of the semiconductor layer in said element region which are not covered with said element isolating insulating film~~ said gate insulating film.

39. (Currently Amended) A semiconductor device according to claim 2, ~~further comprising~~ wherein the gate electrode is a metal gate electrode formed on the gate insulating film, said gate insulating film being formed on a top surface and sides of the semiconductor layer in said element regions which are not covered with said element isolating insulating film, and said metal gate electrode being formed on ~~a top surface and sides of the semiconductor layer in said element region which are not covered with said element isolating insulating film~~ said gate insulating film.